Design Rules Verification Report

Filename : C:\Users\egert\Documents\HH_svn\Trinamic\TMC5130-HBS-REF-R3\TMC513

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Clearance Constraint (Gap=0.3mm) (IsPad and OnMultiLayer and not PadIsPlated),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=2mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.3mm) (Conductor Width=0.2mm) (Air	0
Minimum Annular Ring (Minimum=0.175mm) (All)	0
Hole Size Constraint (Min=0.25mm) (Max=4mm) (All)	0
Hole To Hole Clearance (Gap=0.3mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.07mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.2mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0.2mm) (All)	0
Board Clearance Constraint (Gap=0mm) (OnCopper)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0