Application note: Replacing the TMC236 or TMC246 by the TMC260 or TMC261 in an existing design.

V1.1 – 2011-DEC-02

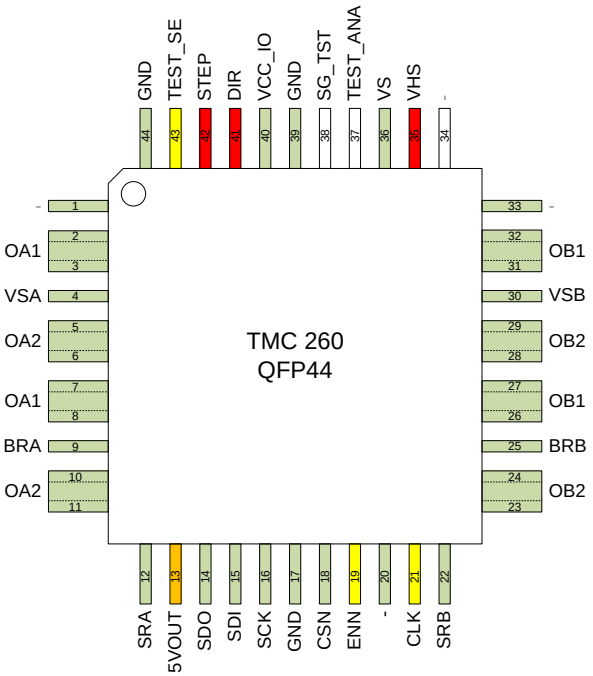
1 Comparing the TMC260 to the TMC236

The TMC260 and TMC261 use the same package as the TMC236 and also the same basic pinning. In order to provide an upgrade path, a TMC236 or TMC246 application can be designed in a way that an application can support both, the TMC260 and the TMC236 or TMC246 in one footprint. Therefore it is important to understand the differences.

Differences to TMC236 and TMC246

- Higher microstep resolution
- Higher supply voltage
- Less dissipation in PMOS transistors (higher gate drive, bulk diodes are not used for fast decay)
- Longer shift register with 8 bit DAC resolution for up to 256 microsteps
- Optimized silent mixed decay chopper scheme results in less motor power dissipation and zero comparator offset voltage
- Mixed decay portion can optionally be manually controlled and be adapted for minimum vibration
- Optional Step and Direction interface with selectable microstep resolution
- No analog stand alone mode
- Internal chopper oscillator with digital chopper frequency setting
- Digital slope control using two bits for gate current control
- High side and low side MOSFET gate current can be controlled separately
- Internal +5V regulator as additional feature. Since the TMC260 needs a stable +5V source even in a 3.3V environment, it brings its own +5V regulator.
- Short to GND protection without additional external sense resistor
- Stall detection output
- In step/dir mode, SPI interface can be used for configuration and diagnostics

1.1 Comparing the TMC260 / TMC261 pinning to the TMC236



Unused pin in TMC236

Pin fixed for TMC236 compatibility

Pin function sligthly modified (i.e. ENN is now purely digital)

Pin function different, but same voltage levels (i.e. digital pin in both, TMC236 and TMC256)

Different function and voltage levels

Differences in pin function compared to TMC236

Pin number	Function in TMC236	Function in TMC260 / TMC261
1	ANN (digital input, select analog control mode)	unused, no analog control mode
13	COSC, oscillator capacitor of about 1nF to GND	5VOUT, output of internal +5V regulator, requires 220nF capacitor to GND, supplies internal analog circuitry and low side gate drivers
19	ENN, enable input with VCC/2 threshold	ENN, digital enable input (does not tristate SDO pin)
20	SPE, Selects SPI or analog stand alone mode	unused
21	BL1, blank time selection input	Optional external clock input CLK, tie LOW for internal clock.
33	BL2, blank time selection input	unused
37	unused	Analog test mode output (leave open)
38	unused	stallGuard output
35	VT, short to GND detection resistor input	VHS, high side supply filter capacitor. This pin needs to be connected to VS via a 100nF capacitor
41, 42	INA, INB, analog current control input	Digital STEP and DIR inputs (for standalone mode, optional use for SPI mode)
43	SLP, slope control resistor input tied to GND via external resistor	TEST select input, tie low for normal operation

1.2 Detecting driver type via SPI

For a hardware supporting both TMC236 and TMC260, it is possible to identify which chip is used by the system by sending SPI datagrams and evaluation the answer. The idea is that the TMC236 shift register has only 12 bits rather than 20 bits for TMC260, and thus the input bits are shifted through if you send a longer datagram.
Example

Input (MSB to LSB, transmit MSB first)	Response from TMC236/246	Response from TMC260
11110000 00000000 00000000 →	XXX1XXXX XXXX1111 00000000	XXXXXXXX XX00XXXX XXXX1111

Note: X denotes a bit depending on status flags in the IC and thus is unknown in the response

1. $F00000 → Answer $xx, $xx, $x0: TMC236
   Different answer: TMC260

This detection determines the length of the shift register by using the circumstance, that bits shifted through the driver are not modified. For two drivers in series, the datagram is elongated in the same way to 48 bits. The lower 8 bits in the received datagram can be tested then.

The coil drivers of the TMC236 are not switched on by this method, because the coil control bits become set to zero. For the TMC260 the coil drivers have to be enabled using an additional register.

2 Interfacing the TMC26x to the TMC428 driver via SPI

The TMC26x can be directly controlled via SPI by a TMC428. Configuration of the driver is done via cover datagrams. The TMC428 can control up to three TMC26x this way, but please be aware, that the 60 bit driver chain limits performance at higher velocities due to reduced SPI update rate. Best performance is achieved, when only one motor runs at a time. A microstep resolution of 64 steps can be achieved this way.

Driver configuration chain for each driver:

```
10 10 06 05 04 03 02 01
00 10 10 0E 0D 0C 0B 0A
09 08 10 30
```

Set SPI cover length to 20. Set LSMD and cover position accordingly, e.g. both to 0 for one driver, only. Send all configuration datagrams as cover datagrams before operation. The cover datagrams are written right aligned (LSB to LSB) into the cover datagram register of the TMC428.

Send for example $EF090 to enable SPI operation (bit 7 is important to be set). You find an example for the other settings in the TMC262 documentation. In order to reset driver errors, set the motor current to 0 and to the desired value again afterwards.