

AN005: IC Package / PCB Footprint Guidelines - QFN32 5x5

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This application note is meant to be a practical guideline for a specific TRINAMIC IC package and its PCB footprint. The document covers package dimensions, example footprint and general information on PCB footprints.

Contents

1	Figures Index	1
2	Tables Index	1
3	Overview	2
4	QFN32 5x5 Package Details	2
4.1	QFN32 5x5	2
4.2	Dimensions	3
4.3	Land Pattern	4
5	General PCB Footprint Information Resources	5
5.1	QFP Packages	5
5.2	QFN Packages	5
5.3	FBGA Packages	6
5.4	IPC-7351B Standard and Land Pattern Calculator Tool	6
5.5	Disclaimer	7
6	Revision History	7
1	Figures Index	
1	QFN32 (5x5mm) example	2
2	QFN32 (5x5mm) package outline drawings	3
3	QFN32 (5x5mm) example land patterns	4
4	EIA Standard Board Layout of Soldered Pad for QFP Devices (unit: mm)	5
5	Board Layout of Soldered Pad for QFN Devices according to Intersil TB389	6
6	EIA Standard Board Layout of Soldered Pad for FBGA Devices (unit: mm)	6
2	Tables Index	
1	QFN32 (5x5mm) dimensions (unit: mm)	4
2	EIA Standard Board Layout of Soldered Pad for QFP Devices (unit: mm)	5
3	Document Revision	7



3 Overview

This application note is meant to be a practical guideline for a specific TRINAMIC IC package and its PCB footprint. The document covers package dimensions, example footprint and general information on PCB footprints.

An overview of all available combinations of TRINAMIC IC products and package options is given in application note "AN048: Overview of TRINAMIC ICs, Available Packages, and Order Code".

4 QFN32 5x5 Package Details

4.1 QFN32 5x5

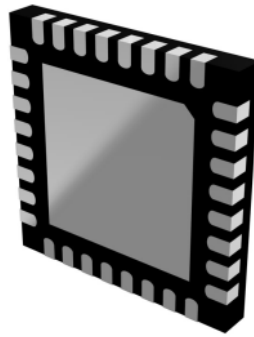


Figure 1: QFN32 (5x5mm) example



4.2 Dimensions

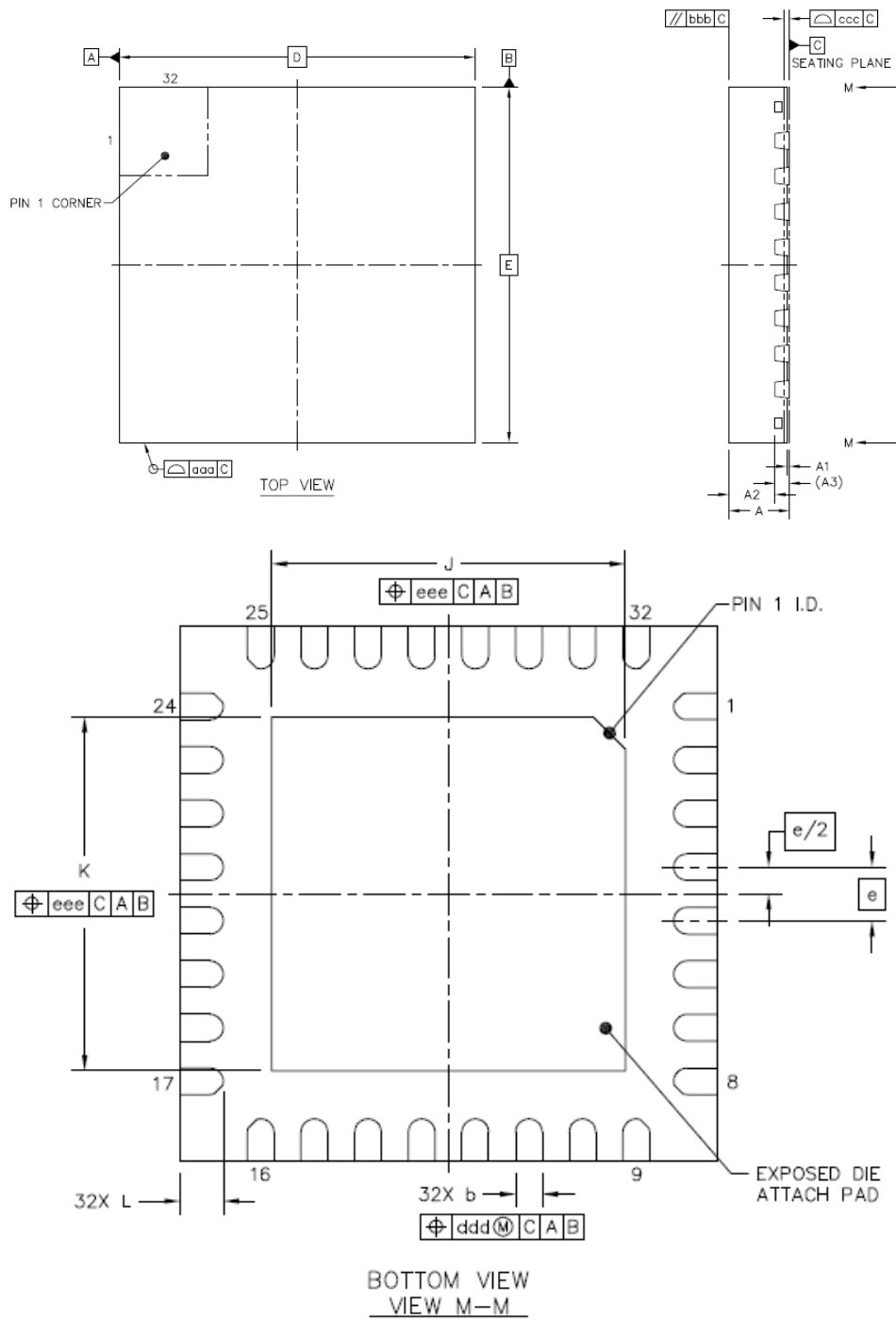


Figure 2: QFN32 (5x5mm) package outline drawings



Symbol	Dimensions in MILLIMETERS			Dimensions in INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.8	0.85	0.9	0.0315	0.0335	0.0354
A1	0	0.035	0.05	0	0.0014	0.002
A2	-	0.65	0.67	-	0.0256	0.0264
A3	0.203 REF			0.0078 REF		
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	5 BSC			0.1969		
E	5 BSC			0.1969		
e	0.5 BSC			0.0197		
J	0.32	0.33	0.34	0.0126	0.013	0.0134
K	0.32	0.33	0.34	0.0126	0.013	0.0134
L	0.35	0.4	0.45	0.0137	0.0157	0.0177
aaa	0.1			0.0039		
bbb	0.1			0.0039		
ccc	0.08			0.0031		
ddd	0.1			0.0039		
eee	0.1			0.0039		

Table 1: QFN32 (5x5mm) dimensions (unit: mm)

4.3 Land Pattern

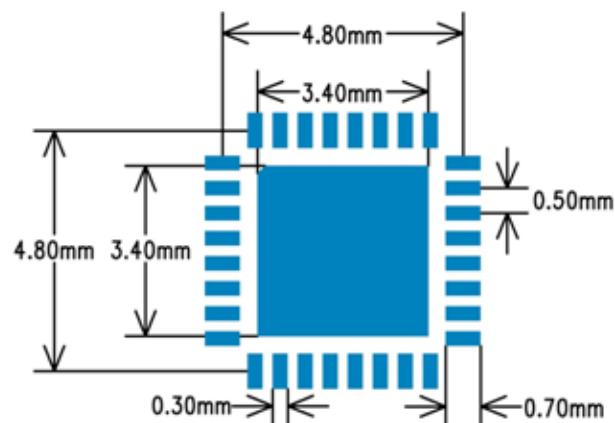


Figure 3: QFN32 (5x5mm) example land patterns



5 General PCB Footprint Information Resources

These guidelines and information are proposals and suggestions as they are proven and work well with TRINAMIC modules.

5.1 QFP Packages

These guidelines are for Quad Flat Packages in general (PQFP, LQFP, TQFP) and are derived from the EIA/JEDEC standard.

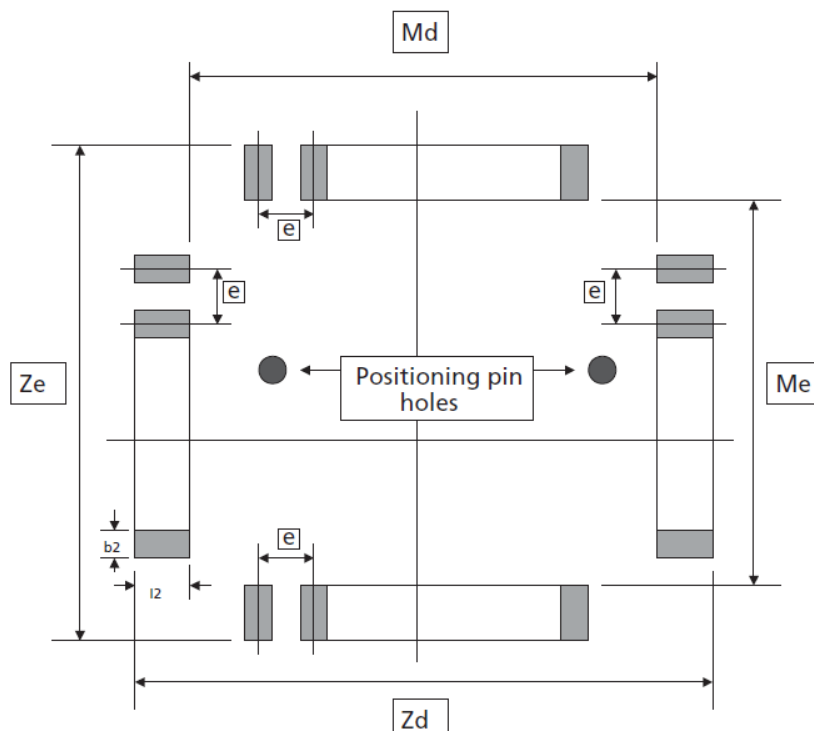


Figure 4: EIA Standard Board Layout of Soldered Pad for QFP Devices (unit: mm)

Dim.	PQ100	PQ144	PQ160 3.2mm	PQ160 3.9mm	PQ/ RQ208	PQ/ RQ240	VQ80	VQ/ TQ100	VQ128	VQ176	TQ64	TQ144	TQ176
Md	20.4	28.4	28.4	29.2	28.2	32.2	13.8	13.8	13.8	19.8	10.1	19.8	23.8
Me	14.4	28.4	28.4	29.2	28.2	32.2	13.8	13.8	13.8	19.8	10.1	19.8	23.8
e	0.65	0.65	0.65	0.65	0.5	0.5	0.65	0.5	0.4	0.4	0.5	0.5	0.5
b2	0.3-0.5	0.3-0.5	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.5	0.3-0.4	0.25- 0.30	0.25- 0.30	0.3-0.4	0.3-0.4	0.3-0.4
l2	1.8	1.8	1.8	1.8	1.6	1.6	1.8	1.6	1.6	1.6	1.6	1.6	1.6

Table 2: EIA Standard Board Layout of Soldered Pad for QFP Devices (unit: mm)

5.2 QFN Packages

These are basic guidelines for Quad Flat No Leads Packages (QFNs). They are derived from the Technical Brief TB389 from Intersil (<http://www.intersil.com/data/tb/TB389.pdf>).



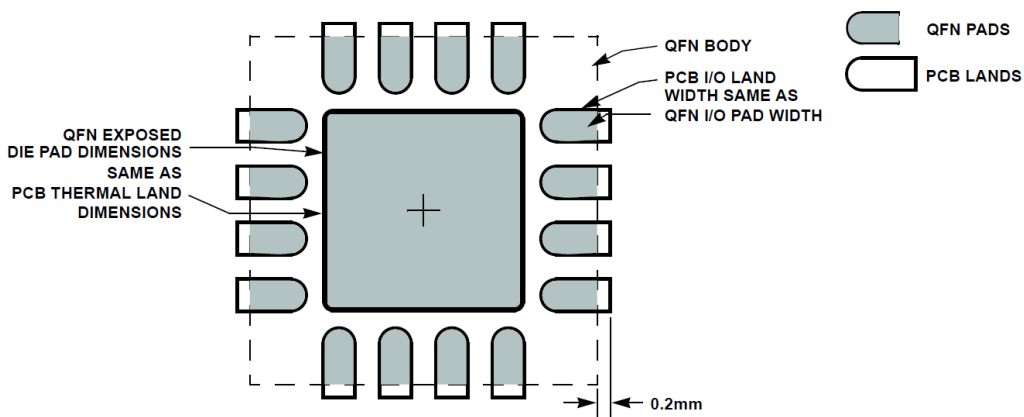


Figure 5: Board Layout of Soldered Pad for QFN Devices according to Intersil TB389

5.3 FBGA Packages

These guidelines are for Fine Line Ball Grid Arrays (FBGAs) with 1mm ball pitch and are derived from the EIA/JEDEC standard.

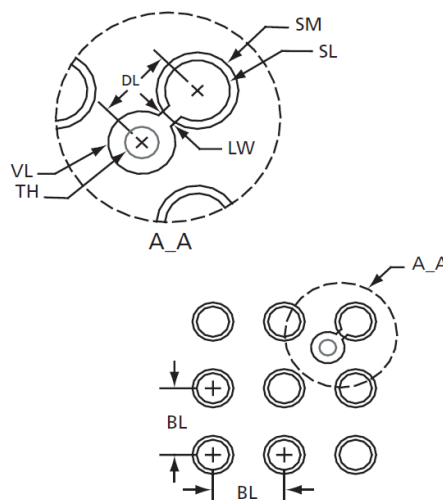


Figure 6: EIA Standard Board Layout of Soldered Pad for FBGA Devices (unit: mm)

5.4 IPC-7351B Standard and Land Pattern Calculator Tool

The IPC-7351B Land Pattern Calculator is based upon algorithms and engineering goals established in the IPC-7351B standard. Mentor Graphics provides a similar free tool. The IPC-7351B standard as well as the Calculator Tool are available online:

<http://www.ipc.org/ContentPage.aspx?pageid=Land-Pattern-Calculator>

<http://www.mentor.com/products/pcb-system-design/library-tools/lp-wizard/lp-viewer-download>



IPC-7351B Description (Source: IPC Online Store, <https://portal.ipc.org/Association/Index.htm>):

“IPC-7351B includes both the standard and an IPC-7351B land pattern calculator for accessing component and land pattern dimensional data. The calculator includes the document’s mathematical algorithms so users can build a land pattern for a corresponding surface mount part quickly and accurately. The tool also allows for modification of dimensional attributes of IPC approved land patterns.

This popular document covers land pattern design for all types of passive and active components, including resistors, capacitors, MELFs, SOPs, QFPs, BGAs, QFNs and SONS. The standard provides printed board designers with an intelligent land pattern naming convention, zero component rotations for CAD systems and three separate land pattern geometries for each component that allow the user to select a land pattern based on desired component density.

Revision B now includes land pattern design guidance and rules for component families such as resistor array packages, aluminum electrolytic capacitors, column and land grid arrays, flat lead devices (SODFL and SOTFL) and dual flat no-lead (DFN) devices. The revision also discusses the usage of thermal tabs and provides a new padstack naming convention that addresses the shape and dimensions of lands on different layers of printed boards.

Purchasers also receive a 30-day trial of the IPC-7351 Land Pattern Wizard developed by Mentor Graphics, which is an advanced version of the IPC-7351B Land Pattern Calculator. The IPC-7351B Land Pattern Wizard tool enables users to not only save their land patterns within new land pattern library files, but also to instantly export land patterns to their preferred CAD format, such as Allegro, Board Station, Expedition, PADS, CADSTAR, OrCAD, Pantheon and P-CAD. 102 pages. Released June 2010.”

5.5 Disclaimer

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6 Revision History

Version	Date	Author	Description
V1.00	20.05.2017	SK	V1.00 release version

Table 3: Document Revision

