Application note:
PCB-Design
Good Ground Connections

TRINAMIC® Motion Control GmbH & Co. KG
GERMANY

www.trinamic.com

This application note is meant to be a practical guideline for the critical aspect of ground connections in PCB layouts using TRINAMIC stepper motor driver ICs.

1 Table of contents

2 Ideal and real world

In an ideal circuit, only components show their specified and no parasitic characteristics and PCB traces have no resistance, inductance or capacitance.
In the real world this is not the case. PCB traces have parasitic properties that could severely influence precise current sensing signals.
The resistance of an usual PCB trace of 35µm copper at 25°C is approximately 0.5mΩ/square. This means a trace that is 0.2mm wide and 10mm long has a resistance of 10mm/0.2mm×0.5mΩ = 50×0.5mΩ = 25mΩ.
The inductance of a trace without a ground plane is approximately 6nH/cm, which can be reduced to approximately 1.2nH/cm by adding a ground plane. The trace from the previous example with a length of 10mm has an inductance of 6nH without or 1.2nH with a ground plane.

2.1 Ideal circuit

The ideal circuit consists of the TMC260 with integrated bridge transistors and two external sense resistors. Additional components are omitted for clarity.

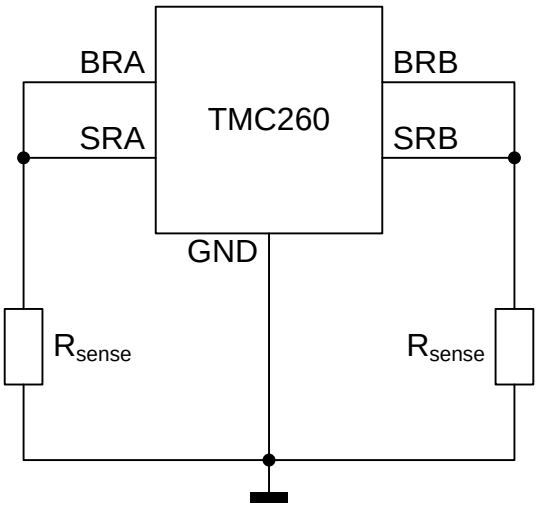

Figure 1: Ideal circuit

The current from the bridges flows from BRA and BRB through the two sense resistors to GND, the voltage on SRA and SRB is measured with reference to GND to control the currents through the two motor phases. In this ideal case, no parasitic effects have an influence on the voltages seen at SRA and SRB.

2.2 Real circuit

In the real circuit, the parasitic properties of the layout and the components have an influence on the accuracy of the sense voltages seen by the TMC260 and the actual voltages across the sense resistor.
The examples explain only the problems introduced by parasitic resistances which appear even with pure DC signals. The parasitic inductances should also be kept as low as possible as their influence shows with dynamic signals which are present due to the chopper current control of the motor driver ICs. Also the parasitic properties of the IC leads and bond wires are not regarded here.

Please note that the layout examples for the TMC260 below are just examples to explain the problems in the design and should not be copied for designs. They also do not include the necessary capacitors which must be placed as close to the IC as possible.

2.2.1 Bad example

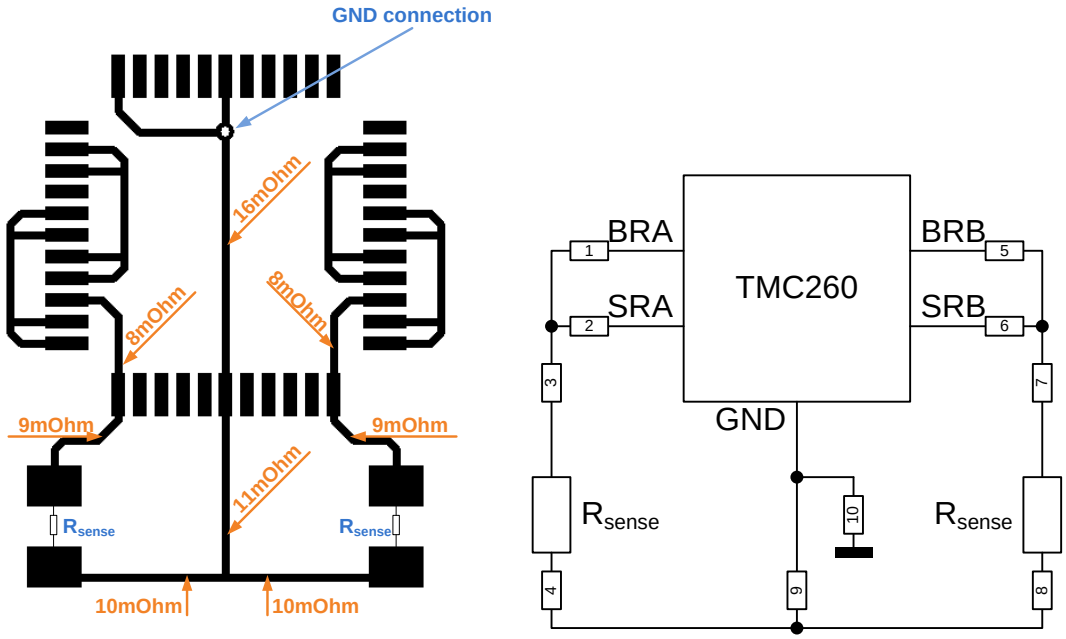

Figure 2: Example for a bad layout

In Figure 2 a bad layout and the corresponding schematic with the parasitic resistances is shown. Parasitic capacitances and inductances are omitted as well as the resistances of the TMC260 pins and internal bonding wires. The parasitic resistances 2 and 6 are zero Ohm in this layout example. The sense voltages measured by the TMC260 (SRA-GND and SRB-GND) not only depend on the phase currents coming out of BRA and BRB and the sense resistor values but also on the parasitic resistances 3 and 4 for phase A, 7 and 8 for phase B as well as 9 for both phases. The voltage at the GND pin also is not 0V in any case but depends on the phase currents, the supply current of the TMC260 and the value of the parasitic resistance 10.
The long ground traces between the SRA/SRB pins and the GND pin cause an additional resistance of 30mOhm, which can increase the value of the sense resistor by a relevant amount.

If the trip voltage of the TMC260 is set to high sensitivity (165mV nominal) and 120mOhm sense resistors have been chosen to reach a peak current of 1.375A, these additional 30mOhm add 25% to the chosen value, reducing the peak current to 1.1A.

Also the common ground path across the resistance 9 causes a dynamic problem as a change in one phase current also influences the measured current of the other phase. The parasitic inductances of the traces have not been taken into account in this example but they also cause problems like distortions of the current waveform.
Another problem with this layout are the thin traces which are capable of carrying the desired current but they increase the resistances and cause unnecessary power losses.

Optimization of the layout consists of three important steps:

1. Reduce the parasitic serial resistances and inductances in the phase current paths
2. Keep the current carrying traces (BRA/BRB to sense resistor) separated from the traces to the sense inputs (SRA/SRB)
3. Keep the current paths from the sense resistors to GND separated from the current path from the IC to GND

Solutions:

1. The traces responsible for the resistances 3, 4, 7 and 8 should be as short as possible. For 4 and 8 the best way is a direct connection to a ground plane with multiple Vias. Also the trace width should be increased where possible.
2. Separate traces for carrying the motor current and measuring the voltage drop across the sense resistor create a Kelvin connection.
3. Direct ground plane connection (as in step 1) keeps the current paths separated

2.2.2 Good example

The performance of the current measurement improves after changing the layout to this:

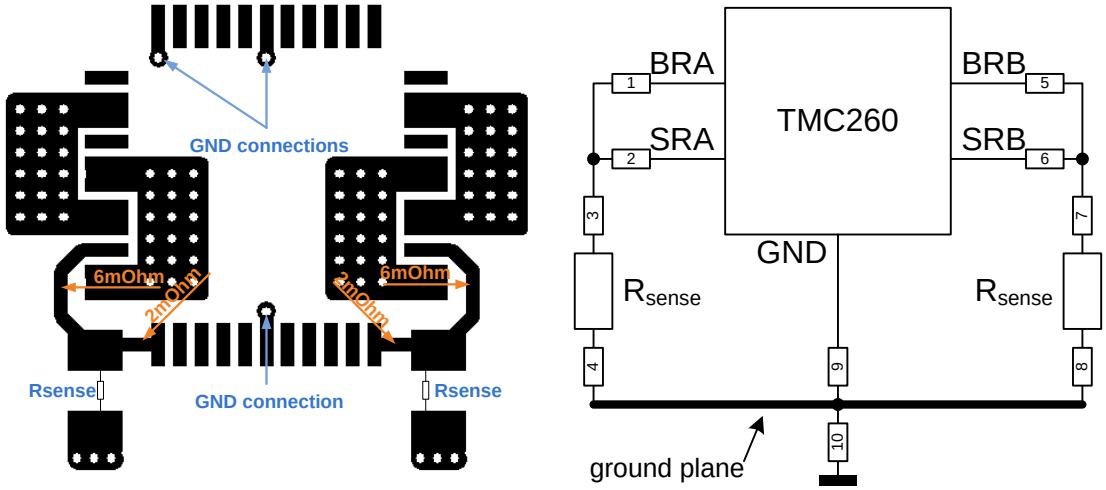

Figure 3: Example for a good layout (ground plane is not shown in the layout)

The serial resistances 3 and 7 are reduced to a minimum by moving the sense resistors closer to the IC and keeping the connection from the sense resistor to the SRx pins out of the current path. The resistances 4 and 8 are reduced by a direct connection from the sense resistors to the ground plane using 3 vias for each resistor.
The reduction of the resistances 1 and 5 doesn't influence the measured voltage drop but improves the overall performance by reducing the power losses in the traces, the parasitic inductance and the risk of interference.

The thick connections of the bridge outputs with 18 vias each are a good practice to dissipate the heat of the internal bridge transistors into the board. This high number of vias is not necessary to carry the motor current as this is limited by the transistors in the TMC260 but the amount of copper helps to spread the heat through all layers of the PCB for applications near the limit of the TMC260 (2A).

2.3 How many copper layers?

While a two layer layout is possible, a four layer layout is recommended.

On a two layer layout, the routing of the ground traces but also of the supply traces has to be planned extremely carefully to avoid common ground paths or high inductances in traces that carry fast changing currents like the bridge supply (i.e. VSA and VSB on the TMC260/TMC261)
The two extra layers in a four layer PCB allow the use of a continuous ground plane, a supply plane and easier and more compact routing of the control signals.
Additionally solid copper layers conduct heat very well and help to keep the temperatures of the power components low.

3 Example layout for a TMC262

An example layout using a TMC262 with external MOSFETs (SO8 package) and the necessary capacitors is shown here. Only the values of the external capacitors are given, their voltage ratings are selected to support the full supply voltage range of the TMC262. The motor outputs are not routed to a connector but shown as short wide tracks on the top layer (Figure 7). All control lines - SPI, Enable, Clock Step/Direction, stallGuard are routed to the bottom of the images on the bottom layer and the top layer (Figure 4, Figure 7Figure 8).
The traces from the MOSFETs to the sense resistors (Y-shaped traces in Figure 5) have slightly different lengths but as they are thicker than the normal traces, the difference is only about 3.2 squares which is equivalent to a resistance of 0.0016 Ohm.

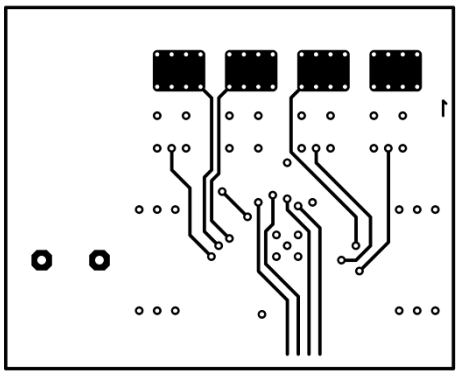

Figure 4: Bottom layer

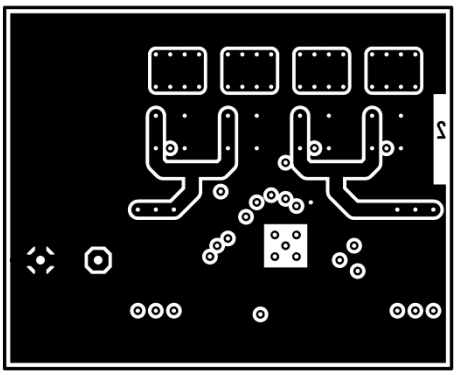

Figure 5: Inner layer (Supply)

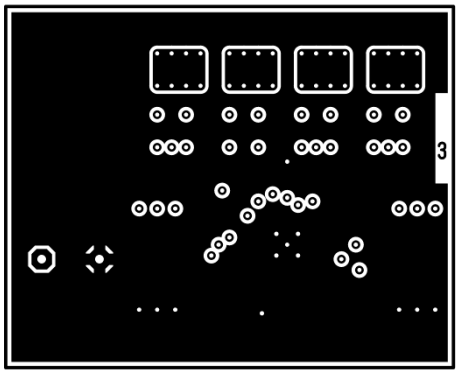

Figure 6: Inner layer (GND)

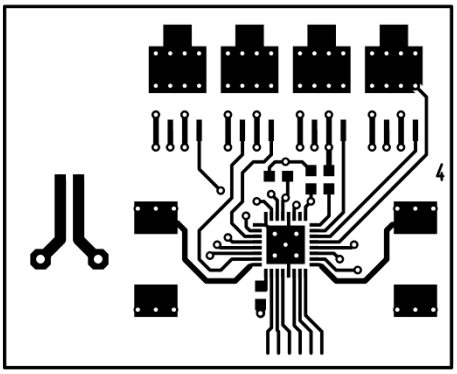

Figure 7: Top layer

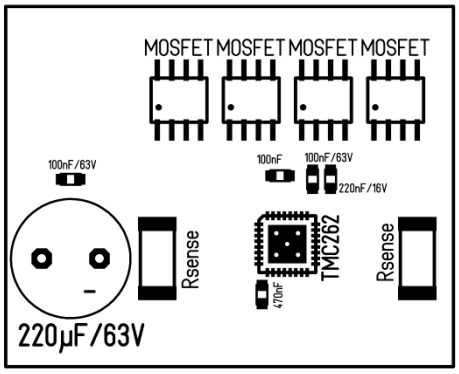

Figure 8: Placement

The five vias in the center pad of the TMC262 are not only used for a low resistance ground connection of the IC but also to transport and spread heat to the GND layer.
The drain connections of the MOSFETs (motor outputs) are connected to solid areas on all four copper layers to allow better heat dissipation.

4 Revision history

4.1 Documentation revision

Version	Date	Author SL=Simon Langhof	Description
1.0	2012-FEB-20	SL	First version

table 1: Documentation revisions